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# Enabling Protocol Validation of High Speed Serial Links using SerDes to transfer data between PHY Chip and Link layer on FPGA

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# Motivation

- High Speed SerDes (PHY) IPs require Silicon validations for every technology node/Foundry with Controller subsystem
- This is done with PHY implemented on specific Chip and Controller logic on FPGA connected through General Purpose IOs (GPIOs)
- Ever increasing data transfer rates lead to explosion in number of GPIO-Pads to transfer data between PHY Chip and FPGA
- Proposed solution of **using Serdes** instead of GPIOs will help to:
  - **Reduce** the SerDes PHY Chip pin count (digital GPIOs)
  - **Reduce PHY Chip size and cost** which is directly related to number of GPIO pads in PAD limited Silicon Chip
  - Address **future requirements** of Silicon validation of higher bit rate Serial links with Controller

# Original Solution

- Serial data on Main Link is converted to parallel digital data in DUT SerDes
- This parallel Data is source synchronously transferred to FPGA through Parallel GPIOs at highest supported bandwidth
- Further increase in data rate requires higher number of GPIOs, which will increase chip area and cost

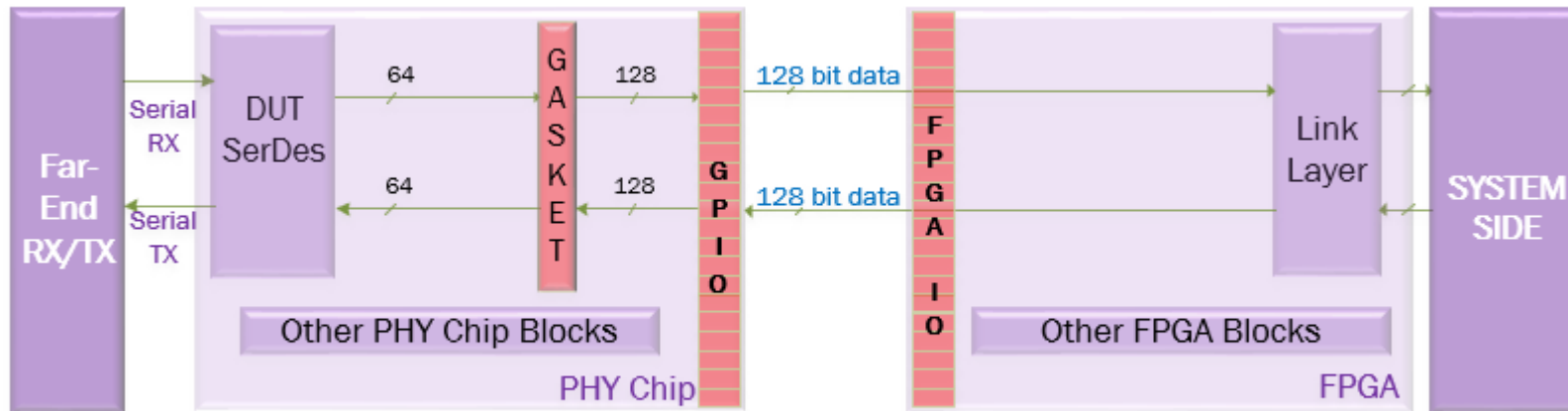


Fig (a): PHY Chip and FPGA with original solution

# Main Idea - 1/2

- Use **multiple lanes of lower rate SerDes** to transfer data between PHY Chip and FPGA instead of large number of GPIOs
- Achieved by **creating a proprietary protocol** without affecting intended main link communications and performance

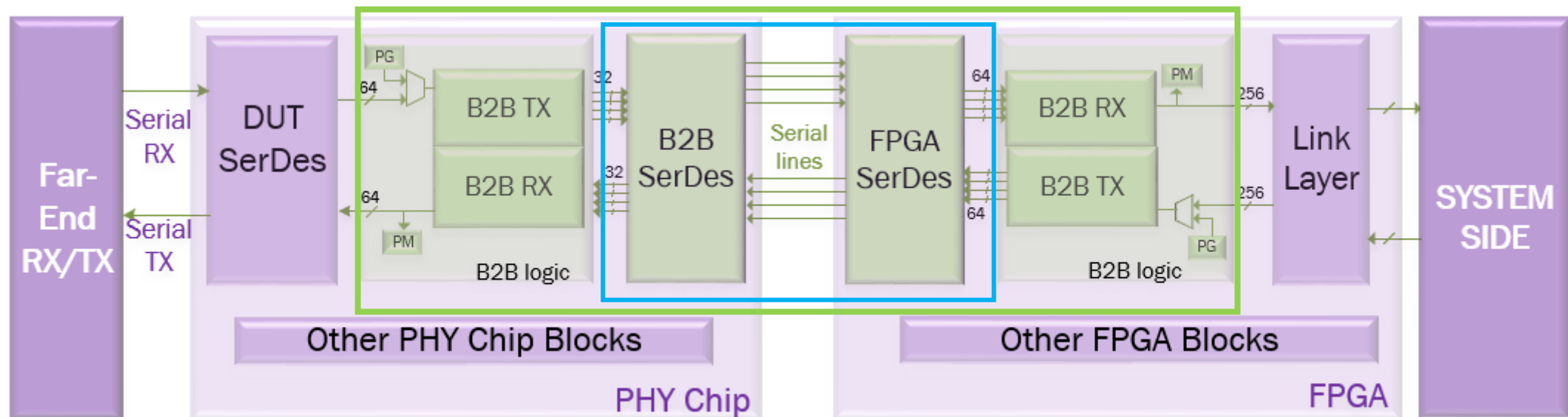


Fig (b) PHY Chip and FPGA with proposed B2B solution

# Main Idea - 2/2

- To support this PHY Chip will additionally include (marked green in fig b)
  - B2B (Back-to-Back) SerDes
  - B2B logic
- FPGA will use embedded SerDes and additional B2B logic similar to PHY Chip to transfer data
- This B2B logic consists of Transmitter path and Receiver path both in PHY Chip and FPGA

# Considerations in designing B2B protocol

- TX

## Word Stuff

Variable word stuffing based on main link rate (2.5 – 64Gbps) to match B2B link rate

## Data Demux

Data distribution across active lanes of B2B link

## Scrambler

Main link payload scrambling and high transition idle symbol insertion to keep B2B link CDR locked

## SOB/EOB Insert

Start of Burst and End of Burst insertion to differentiate payload of main link from idle symbol on Rx side

- RX

## Word Aligner

Re-align data word boundaries, lost due to serialization and de-serialization

## De-skewer

Compensate skew introduced among different lanes of B2B link to prepare data aggregation

## De-Scrambler

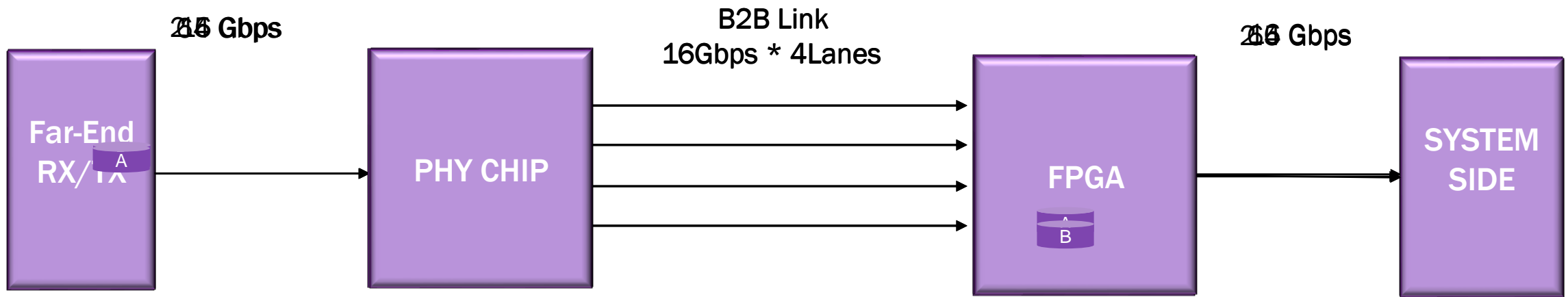
Aggregate data from all lanes of B2B to single payload with de-scrambling

## Word Destuff

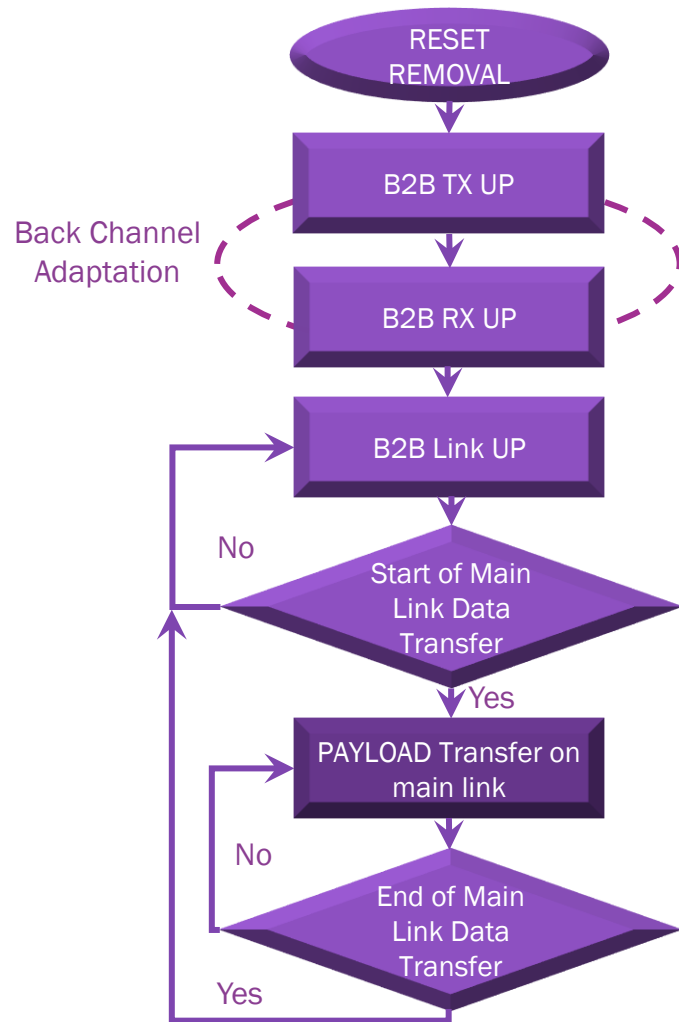
Remove all TX inserted Idle patterns, SOB, EOB and stuffed words

# Data Transfer

- To support maximum throughput of 64gbps of main link, 4x16gbps lanes of B2B link are used
  - These 4 lanes continue to operate on constant 16gbps rate irrespective of main link data rate
  - This is achieved by using variable bit stuffing techniques



# Bring-up Sequence



- This sequence ensures **start-up latency** of main link is not impacted as:

- B2B link is brought up before main link is established
- B2B link CDR locking and data channel adaptation is performed
- B2B link remains in active state irrespective of main link state

# Evidence

- The logic is implemented with
  - PCIe6 PHY Chip
  - Xilinx FPGA Transceiver model (Virtex UltraScale+ XCVU19P)
- With proposed B2B solution at 64Gbps max bitrate,
  - Multiple **PHY Silicon Chips** across different technology nodes are taped out
  - PHY Silicon Chip pin reduction is illustrated in table below

Max Bit Rate (Gbps)	Number of GPIOs for data transfer (Original Solution)	GPIOs Max Freq (MHz) (Original Solution)	Number of Analog Pads (DP,DN) (B2B Solution)	B2B Serial link Rate (Gbps) (B2B Solution)	Min PHY Chip pins Saved
64	128 TX + 128 RX	500	8TX + 8RX	16	240
128	256 TX + 256 RX	500	16TX + 16RX	16	480
128	256 TX + 256 RX	500	8TX + 8RX	32	496

# Summary

- Proposed B2B solution enables protocol validation **agnostic to main link protocol and technology nodes**
- **80%+ reduction in PHY Chip pin-count at 64gbps**
  - Using this technique, **16 analog pads are sufficient instead of 256 digital GPIOs**
- **35% reduction** in PHY Chip area
- Simplifies Interface timing closure between PHY Chip and FPGA
- **Address future requirements** of Silicon validation of higher bit rate Serial link PHY with Controller



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# Thank You

